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(54) Method of fabricating gate stack having a reduced height.

(57) An integrated circuit device having reduced-height gate stack is fabricated by using a patterned oxide hard mask (20) to pattern the underlying metal layer (18). The oxide mask is removed and the patterned metal is subsequently used as a mask to etch the polysilicon layer (16).

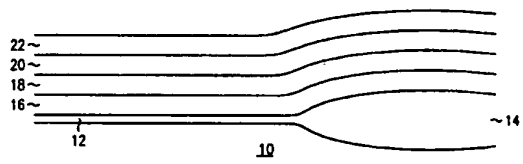

FIG. 1

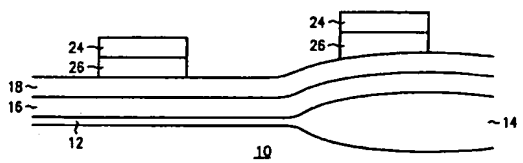

FIG. 2

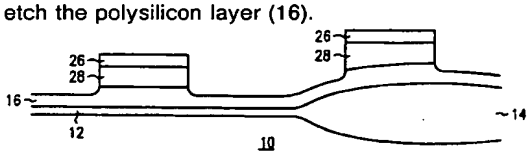

FIG. 3

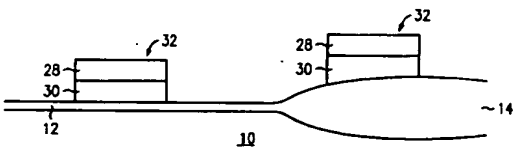

FIG. 4

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Field of the Invention

This invention generally relates to the fabrication of integrated circuits, and more particularly to a method for fabricating multilayer gate stacks in an integrated circuit.

Background of the Invention

A gate stack or multilayer structure is typically used as gate electrodes or interconnects in MOS and CMOS integrated circuits. One gate stack that has been proposed consists of layers of doped polysilicon or amorphous silicon, tungsten silicide (WSi_2), and silicon dioxide (SiO2). The oxide layer is patterned and used as a hard mask to subsequently etch the underlying polysilicon and silicide layers. After the gate stack is patterned in this manner, the oxide hard mask is retained in the final gate structure. Consequently, the total height of the gate stack includes the height of the oxide mask layer, which contributes as much as 30 % to the total height of the gate stack.

The oxide mask layer cannot be removed after the gate stack is patterned since its removal would also thin down the field oxide layer and thus adversely affect isolation between adjacent transistors. Because both the oxide mask and the field oxide layer are oxides, the etching selectivity between them is poor. Thinning down the field oxide layer can also cause significant damage which can result in defects in the integrated circuit.

Different ways of reducing gate-stack height have been attempted, but have not proven to be successful in terms of cost effectiveness as a result of low yield. One approach has involved the use of a BPTEOS hard mask with a special wet etch. One problem with the use of BPTEOS as a hard mask has been an attack on the field oxide layer due to the increase in the wet etch rate during the removal of the hard mask, especially at the edges of the field oxide, where the wet etch rate is especially high. A further problem in this approach is the tendency of boron and phosphorous impurities in the oxide to diffuse rapidly.

Previous proposals to avoid the use of oxide hard mask have failed to control the transistor dimensions with the required precision and suffer from poor linewidth control as a result of deposits formed on the patterned vertical sidewalls. In the larger pattern geometries, deposits of 100 to 200 Angstroms did not present serious problems; however, in the new generation of smaller pattern geometries, the resultant poor linewidth control may result in defective transistors or low yield.

Summary and Objects of the Invention

It is an object of the present invention to provide a process of fabricating an integrated circuit with a gate-stack structure having reduced topography.

It is another object of the invention to provide a process for fabricating integrated circuits in which the hard oxide mask of a gate stack structure can be removed by a single and reliable process.

A reduction in the height of a gate stack is achieved in accordance with the present invention by removing the silicon dioxide mask layer, leaving only a metal layer and a polysilicon layer in the final gate stack. The oxide hard mask used to pattern the metal layer may be removed since the polysilicon layer is used to protect the field oxide layer from the etchant used to selectively remove the oxide mask. The etching is completed using the patterned metal as a mask to etch the polysilicon layer down to the gate oxide, without thinning down the field oxide layer. Advantages of the process include reduction of topography, process uniformity, and simplicity as compared to the conventional gate fabrication processes.

Brief Summary of the Drawings

The foregoing features of the present invention can be more fully understood from the following detailed description of a specific illustrative embodiment thereof, presented hereinbelow in conjunction with the accompanying drawing, in which FIGS. 1-4 illustrate cross-sectional views of an integrated circuit at successive stages of its fabrication in accordance with the invention.

Detailed Description of the Invention

Referring to FIG. 1, the fabrication of the gate stack in accordance with the invention begins with a silicon substrate 10 on which is formed, as is conventional, a gate oxide layer 12 and a surrounding field oxide layer 14, the latter providing isolation between adjacent transistors. A layer of doped polysilicon 16 or amorphous silicon is formed over the oxide layers 12, 14 and a refractory metal layer 18 such as of tungsten silicide (WSi_2) or titanium nitride (TiN) silicide is formed over polysilicon layer 16. A silicon dioxide layer 20 is formed over metal layer 18 and a layer of photoresist 22 is formed over the oxide layer 20. Layers 16 and 18 and 20 may each be about 1000Å in thickness.

Next, as shown in Fig. 2, as is conventional, the photo-resist layer 22 is patterned by a photolithograph process to form photoresist masks 24, and the underlying silicon oxide layer 20 is etched away to leave a patterned layer 26 of silicon diox-

ide beneath the patterned photoresist 24.

Thereafter, as shown in Fig. 3, the photoresist masks 24 are removed in a conventional manner. In accordance with the present invention, the now-exposed patterned oxide layer 26 is employed as a hard mask to etch away the exposed metal layer 18 to leave a patterned layer of metal 28, and also partly to etch away the exposed polysilicon layer 16.

If the metal layer and the polysilicon layer have significant etching selectivity, etching the metal layer can stop upon reaching the upper surface of the polysilicon layer. A portion of the polysilicon layer 16 will be etched away by an amount determined by the etching selectivity.

Following the selective etching of the metal layer, the oxide hard mask 24 is removed completely by a known technique, as shown in Fig. 4, which may include either dry etching or wet etching. During the removal of the hard mask, the remaining polysilicon layer 16 is of sufficient thickness to protect the field oxide layer 14 from the etchant used in this step of the process. The now-exposed patterned metal silicide layer 28 is then used as a hard mask for etching away the remaining polysilicon layer 24, as shown in Fig. 4, to form a patterned polysilicon layer 30 to the gate oxide layer 12. This etching step can be safely performed without attacking the gate and field oxide layers because the etching selectivity of the polysilicon layer to the oxide is high, about 20 to 1.

As shown in Fig. 4, the process produces a gate stack 32, comprising the patterned polysilicon layer 30 and the patterned metal layer 28, as opposed to a conventional gate stack, which also includes an overlying oxide layer. The gate stack fabricated in this manner simplifies the back-end process of wiring and the like as a result of the reduced height of the gate stack. The gate stack, as shown in Fig. 4, may constitute the gate electrode of an MOS transistor or an interconnect located in the field region.

The above-described process is merely illustrative of the principles of the present invention. Numerous modifications and adaptations thereof will be readily apparent to those of ordinary skill in this art without necessarily departing from the spirit and scope of the present invention.

Claims

1. A process of fabricating a gate stack in an integrated circuit including the steps of:
   a) forming a polysilicon layer on a substrate,
   b) forming a refractory metal layer over said polysilicon layer,
   c) forming an oxide layer over said metal layer,
   d) forming a photo-resist layer over said oxide layer,
   e) patterning said photoresist layer and said underlying oxide layer,
   f) removing said patterned photoresist,
   g) using said remaining patterned oxide layer as a hard mask, etching away the exposed portion of said metal layer,
   h) removing said oxide hard mask, and
   i) using said patterned metal layer as a mask, etching away the exposed polysilicon layer.

2. The process of claim 1, in which said step of etching the exposed portion of said metal layer also includes the partial etching of the eased polysilicon layer.

3. The process of claim 1, in which said remaining polysilicon layer acts as an etching mask for the field oxide layer during said step of etching said exposed metal layer.

4. The process of claim 3, wherein said metal layer comprises a metal selected from the group including tungsten silicide and titanium nitride.

5. The process of claim 3, wherein said patterned metal mask and said patterned polysilicon layer underlying said metal form a reduced-height gate stack.

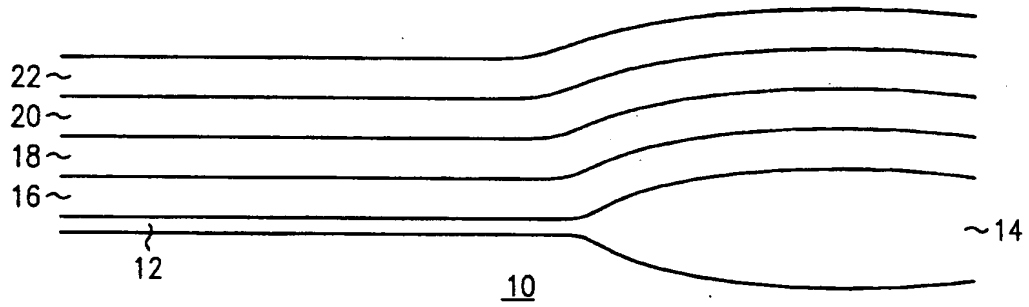

FIG. 1

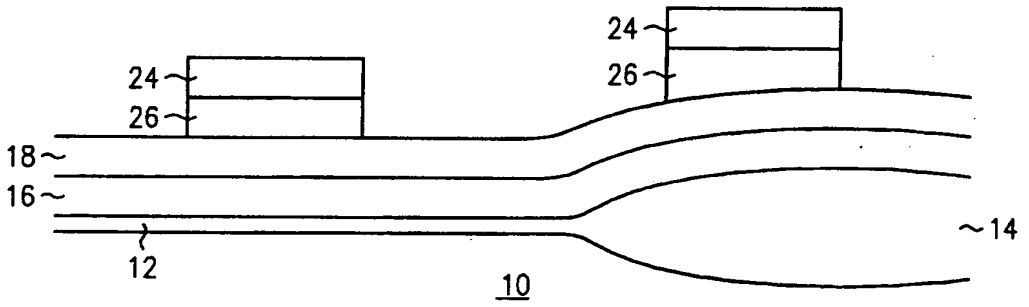

FIG. 2

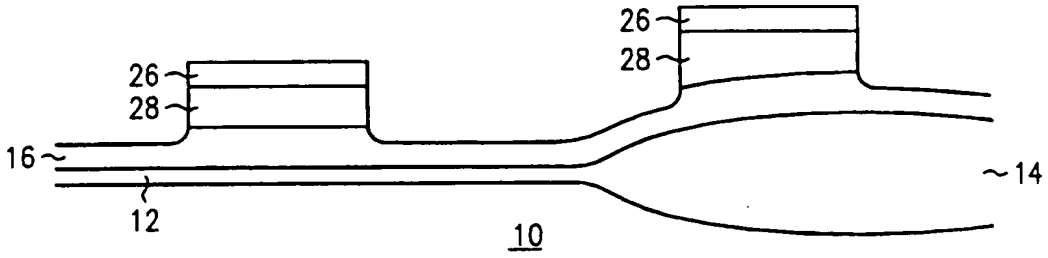

FIG. 3

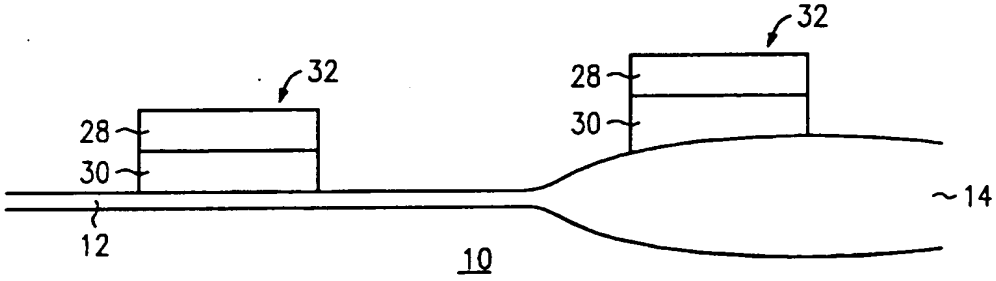

FIG. 4

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 94 30 9348

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
A	US-A-5 094 712 (BECKER DAVID S ET AL) 10 March 1992 * column 5, line 33 * * column 7, line 4 - column 9, line 13; figures * ---	1,4	H01L21/28
A	US-A-4 818 715 (CHAO FUNG-CHING) 4 April 1989 * column 6, line 4 - line 18 * ---	1-3	
A	US-A-4 971 655 (STEFANO JAMES J ET AL) 20 November 1990 * column 3, line 51 - column 4, line 7; figures 1,2,6,7 * ---	1,5	
P,A	DE-A-43 18 688 (MITSUBISHI ELECTRIC CORP) 10 February 1994 * figures 7-11 * ---	1	
A	EXTENDED ABSTRACTS, vol. 87-1,no. 1, 1987 PRINCETON, NEW JERSEY US, page 243 N. LIFSHITZ ET AL * the whole document * -----	5	TECHNICAL FIELDS SEARCHED (Int.Cl.6) H01L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
BERLIN	2 May 1995	Roussel, A

CATEGORY OF CITED DOCUMENTS

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